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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,689	01/02/2002	Marvin J. Rich	POU920010166US1	4133

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,689	RICH ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-2 and 7-15 have been presented for examination based on amendment filed on 14th October 2005.
2. Claim(s) 1, 7, 10, 12 and 15 are amended.
3. Claim(s) 3-6 are cancelled.
4. Previous non-final office action mailed on 14th August 2005 is incorporated within this office action unless otherwise specified where the more current rejection for the amended claims supercedes the previous rejection.
5. The arguments submitted by the applicant have been fully considered. Claims 1-2 and 7-15 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

6. Examiner respectfully withdraws the claim objection(s) to claim(s) 1-6 in view of the amendment and/or applicant's arguments.
7. Examiner respectfully withdraws the claim rejection(s) under 35 USC § 112 ¶1 to claim 3 in view of the amendment and/or applicant's arguments.
8. Examiner respectfully withdraws the claim rejection(s) under 35 USC § 112 ¶2 to claim(s) 1,3,6,7,10,12 and 15 in view of the amendment and/or applicant's arguments.
9. Examiner respectfully withdraws the claim rejection(s) under 35 USC § 101 to claim(s) 1-6 in view of the amendment, cancellation and/or applicant's arguments. Claims 10 & 11 remain rejected despite the amendment to the claim and reasons for the rejects are presented in the 101 rejected ahead in this office action.
10. Examiner maintains the claim rejection(s) under 35 USC § 103 to all remaining claim in view of the amendment and/or applicant's arguments. Please see response below.

Specification

11. Modification to the specification to update the details related to the co-pending applications are accepted.

12. Modification to correct the tuple sequence, on page 22, is also accepted.

Response to Applicant's Remarks for 35 U.S.C. § 103

13. Claim(s) 1-2 and 7-15 were rejected under 35 U.S.C. 103(a) as being unpatentable over various prior art references presented in the previous office action incorporated here by reference.

Regarding Claim 1

Applicant has argued that correlation taught by OVI2.1 reference is limited to single instance of a logic gate. Examiner respectfully disagrees as OVI2.1 clearly states that cell is part of a correlation group and primitives (multiple unique cells in the library) sharing the same correlation are part of the group (OVI2.1: Pg.3-10 "Correlation Entry" ¶1 & last paragraph). The correlation entry, as disclosed in claim 1, is used by each individual cell primitives as shown by OVI2.1 reference (OVI2.1: Pg.3-10, Last paragraph & 3-11 Last paragraph). Further arguments relating to correlation process and analysis are mere allegations and are not part of the claimed subject matter. Further, OVI2.1 teaches correlating disparate & multiple gates primitives in "correlation group". Further arguments, also not claimed, relating to scaling based on chip size are also taught as the correlation is done by percentage values.

Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive. Rejection to claim 1 as disclosed is maintained.

Regarding Claim 10 & 11

Rejections to claims 10 & 11 are also maintained for the same reasons as disclosed above.

Regarding Claim 12

Claim 12 is rejected based on the obviousness. Please see the claim 12 rejection under 35 USC 103 below. Examiner respectfully disagrees with the applicant arguments, which are found to be unpersuasive and the rejection is maintained. Further, for further review the Stanley reference[1], cited but not used in previous office action shows an array of delay values (Stanley: Pg. 28.1.3, "Vital Level 0 Compliance").

Regarding Claim 15

Claim 15 is rejected based on the obviousness. Please see the claim 15 rejection under 35 USC 103 below. Applicant argues that the cited reference does not teach or suggest reduced SDF file or a "super generic". The reduced SDF limitation as such is not claimed. Examiner respectfully disagrees with the applicant arguments, which are found to be unpersuasive and the rejection is maintained.

[1] "Standardizing ASIC Libraries in VHDL Using VITAL: a Tutorial"; Krolikoski S.J.; IEEE 1995 Custom Integrate Circuits Conference.

Regarding Claim 7-9

Applicant has presented similar argument as presented for claim 15 above on page 18 of remarks. Please see response to claim 15 arguments above. Further, applicant has presented similar argument as presented for claim 1. Please see response to claim 1 argument above.

Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive. Rejections to claim 1-2 and 7-15 as disclosed are maintained.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

14. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "computer readable medium", does not reasonably provide enablement for "a storage medium". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make/practice the invention commensurate in scope with these claims. Further, the amended term "a processing medium" also has no antecedent basis in the specification. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claim 11 recites the limitation "a computer readable medium". There is insufficient antecedent basis for this limitation in the claim. Claim 11 is dependent from claim 10 where the above limitation was removed by the amendment. Corrections to claim 11 are required.

Claim Rejections for amended claims - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 1-2 & 10-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Std1076*, in view of *OVI2.1*.

Regarding Claim 1 & 10

Claim 1 rejection as presented in the previous office action is maintained and incorporated here in entirety. The amended clarification to the preamble makes the claimed method useful. The amended limitation of storing "in memory" is obvious as the run time ASIC designs and associated libraries are stored in memory. *The timing generics taught by the prior art are functionally equivalent to the amended "tpd_super_rise" and "tpd_super_fall" generics* (Std1076: at least in Pg. 20 Lines 11-31). A similar amendment was made in claim 10 and the claim 10 is rejected for the same reasons as above.

Regarding Claim 12, 13 and 14

Std1076 teaches binding correlated delay constants in a 3 dimensional variable data array structure to the VHDL library (Std1076: Pg. 23 Lines 15-22; Pg.59-60 Sec 9.1). Although the array disclosed is not 3 dimensional, the 3 axes of the 3 dimensional data array are obvious. The z-axis donates the blocks for given gate topology. There are multiple versions delays for a single gate topology that can be specified based on the conditions command (Std1076: Pg.27-28, Section 5.2.7.2.1 & 5.2.7.3.2). This is equivalent in functionality and would satisfy z-axis parameter. The x-axis parameter represents the delay name. There are various timing generics representing the delay names taught by the **Std1076** (Std1076: pg.12 Lines 1-5).

Std1076 teaches the y-axis, which represents the actual delay value (Std1076: Pg. 25 Lines 1–14). Further, z-axis data structure represents a generic delay name common to plurality of logic gates (e.g. Tipd for a 2 input gate structure) (Std1076: Pg. 25 Lines 1–14).

Further, regarding claim 12, the Std1076 reference with accompanying interpretation provided above clearly teaches a 3 dimensional array structure obvious for delay data storage. The added limitations "using a VHDL package embedded with correlation delay data" where the correlation delay data is embedded in the VHDL package is taught by OVI2.1 (OVI2.1: 3-12 Example).

17. Claim 15 was rejected under 35 U.S.C. 103(a) as being unpatentable over Std1076, in view of Std1481.

Regarding Claim 15

Std1076 teaches storing the rise time and fall time generic declarations for every gate model in VHDL model library (Std1076: Pg.62, Section 9.4.1; Pg.19 Section 5.1/5.2 Lines 24-45). Further, **Std1076** teaches initializing and updating other generic variables in the model (Std1076: Pg.20 Lines 11-13). **Std1076** teaches mapping between specific timing generics and the standard delay format constructs (Std1076: Pg. 20 Lines 16-31) which contain the delay data. *These timing generics are functionally equivalent to the amended "tpd_super_rise" and "tpd_super_fall" generics.*

Further, **Std1076** teaches binding correlated delay constants in a 3 dimensional variable data array structure to the VHDL library (Std1076: Pg. 23 Lines 15-22; Pg.59-60 Sec 9.1). Although the array disclosed is not 3 dimensional, the 3 axes of the 3 dimensional data array are obvious. The z-axis donates the blocks for given gate topology. There are multiple versions delays for a single gate topology that can be specified based on the conditions command (Std1076: Pg.27-28, Section 5.2.7.2.1 & 5.2.7.3.2). This is equivalent in functionality and would satisfy z-axis parameter. The x-axis parameter represents the delay name. There are various timing generics representing the delay names taught by the **Std1076** (Std1076: pg.12 Lines 1-5). **Std1076** teaches the y-axis, which represents the actual delay value (Std1076: Pg. 25 Lines 1–14).

Std1076 does not teach generic declarations consisting of pointer and resolving the pointer at link-time.

Std1481 teaches delay calculation language (DCL) where generic declaration associated to delay data contains pointer (Std1481: Pg.4 Sec 3.20; Pg.20 Cell_Data; Pg.21 Path_Data; Pg.30 Sec 6.7.1). Further, Std1481 teaches resolving the pointer at link time (Std1481: Pg.4 Sec. 3.17).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Std1481** to **Std1076** and handle delays in the disclosed manner. The motivation would to combine would have been that **Std1481** teaches delay calculation pre- and post-layout phases of chip designs done in Verilog and VHDL (Std1481: Pg iii Background ¶ 4). The previously disclosed OVI standard for the SDF files works with **Std1481** and is compatible with DCL (Std1481: Pg iii Background ¶5).

18. Claims 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Std1076, in view of Std1481, further in view of OVI2.1.

Regarding Claim 7

Teachings of and motivation to combine **Std1076** & **Std1481** are disclosed in claim 15 rejections above. Further, **Std1481** discloses a linking procedure involving memory and a computer-aided engineering (or EDA) environment (Std1481: Pg.4 Sec. 3.17, Abstract –Top page). *The timing generics taught by the prior art are functionally equivalent to the amended "tpd_super_rise" and "tpd_super_fall" generics* (Std1076: at least in Pg. 20 Lines 11-31).

Std1076 & **Std1481** do not teach correlation policy.

OVI2.1 teaches correlation policy and format for the delay correlation (OVI2.1: Pg. 3-10 to 3-12).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **OVI2.1** and apply them to **Std1076** & **Std1481** to handle delays in the disclosed form. The motivation to combine would have been that **Std1481** teaches delay calculation for pre- and post-layout phases of chip designs done in Verilog or VHDL (Std1481: Pg iii Background ¶ 4) and works with **OVI2.1.** Also, the previously disclosed OVI standard for the SDF files works with **Std1481** and is compatible with DCL (Std1481: Pg iii Background ¶5). Further, the motivation to combine **OVI2.1** with **Std1076** would have been that **OVI2.1** discloses the Standard Delay Format Standard for the standard delay file generated. **Std1076** uses the standard delay file to back annotate and map the

delays from the SDF file constructs (OVI2.1: Pg. 3-10 to 3-12; Std1076: Pg. 5 Lines 23-25).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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